(2)

Quarterly Progress Report

(October 1, 1993 through December 31, 1993)

on

VLSI for High-Speed Digital Signal Processing

prepared for

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

Scientific Officer: Dr. Clifford Lau

Grant No.: N00014-91-J-1852
R & T Project: 4148503-03

Principal Investigator: Alan N. Willson, Jr.

7400 Boelter Hall
University of California

Los Angeles, CA 90024-1600
(310)825-7400
e-mail: willson@ee.ucla.edu

VLSI for High-Speed Digital Signal Processing

Quarterly Progress Report – 10/1/93 through 12/31/93

During the past quarter we have made considerable progress on the design and layout of the five-processor ring IC, although we missed the deadline for the January 1994 MOSIS 0.8-μm CMOS fabrication run. The next available run has an April 6 deadline, and we hope to have our chip on that run, or at the worst on the following one. We are trying to be as cautious as possible in our fabrication of this rather expensive chip in order to maximize our chances that only one fabrication run will be necessary. As we have mentioned previously, the chip will be a "drop in" replacement for our one-processor chip, which was found fully functional on its first fabrication, and which was described in our previous progress report.

We have also made good progress on our IBM PC boards which are shown in Figs. 1 and 2, and which have been designed to demonstrate the capabilities of our ring processor chip. The two boards, which interface directly to the IBM PC bus, allow for the computer hosting the boards to upload image files for two-dimensional filtering, or a data file for one-dimensional filtering. The first board (Fig. 1) contains four of our ring-processor ICs, a PC bus interface, and several state-machines for control of the data paths. The second board (Fig. 2) contains a large RAM bank for storing images and the necessary blocking and control circuitry for implementing two-dimensional processing using our ring processor chips on the first board. The boards also allow

an external data source to be fed to the processors for higher speed processing. Both boards have been debugged and fully tested. Our last test involved programming a 15-tap FIR filter into one of the four processors on the board. After loading the program and coefficient values, an impulse function was loaded into the memory on the board and it was then used as input to the processor. After running the data through the processor the correct filter coefficients were observed at the processor output.

In parallel with testing the hardware, software development has begun. To support the display of images processed by the ring processors, a routine has been written to display an image in the 256 gray scale mode on a VGA monitor. This will allow images to be displayed before and after 3-D filtering by the ring processors on the boards. Currently work is being done to integrate the testing and debugging software into the final software package used to demonstrate and drive the two boards.

Our paper entitled "An Architecture for High-Performance/Small-Area Multipliers for Use in Digital Filtering Applications" was accepted for publication in the *IEEE J. of Solid State Circuits.* We have now received the page proofs, and a copy is enclosed. This paper describes our work on the multiplier that is used in each processor in our ring chip.

The paper entitled "An Improvement to the Powell and Chau Linear Phase IIR Filters," which describes a new technique that we have developed for improving on the clever method proposed by Powell and Chau for implementing very good approximations to linear phase IIR filters, was accepted for publication by the *IEEE Trans.*

on Signal Processing. An abbreviated version of the paper was also accepted for presentation at the ICASSP '94 conference in Adelaide, Australia. Copies of both papers are enclosed. In addition, work has been progressing nicely on the implementation of a fast FIFO/LIFO chip that will facilitate a board-level implementation (along with our ring processor chip, of course) of the improved Powell and Chau system.

The efficient "prefilter" IC that was mentioned in the last progress report, which is the ONR-supported MS thesis project of Linda Ying, was returned during this quarter from its second fabrication. It was tested and found fully functional up to the maximum (50 MHz) speed of our Tektronix LV500 chip tester. This chip can be used along with our previously implemented programmable FIR chip to realize the Adams-Willson type of prefilter-equalizer cascade structures.

Four of our single-processor ICs
To be replaced later with four of our 5-processor ring ICs.

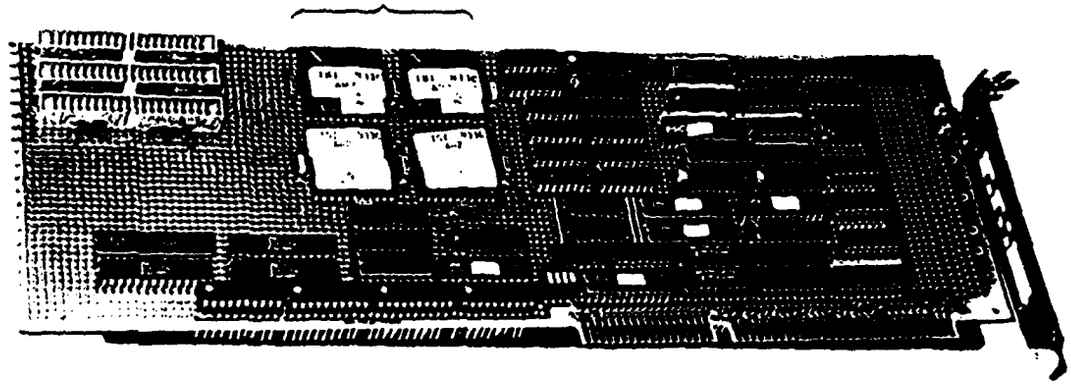

Figure 1. Processor Board

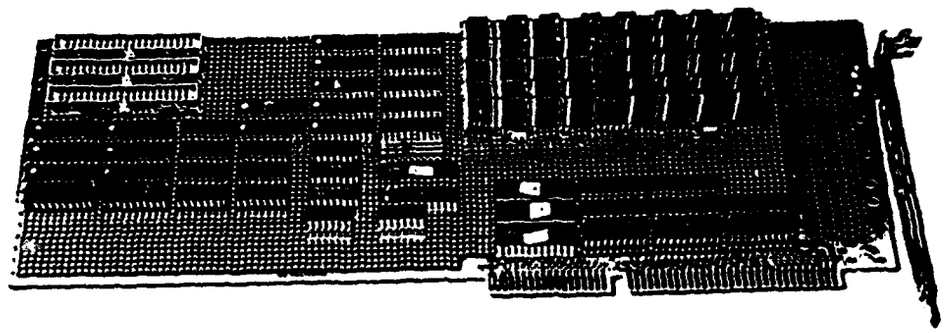

Figure 2. 2-D Filtering Board